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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,083	09/19/2003	Boris Prokopenko	372465-01001	8438

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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,083	PROKOPENKO ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003 and 13 February 2004 a*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 09/19/2003, Declaration on 02/13/2004, and Drawings on 05/17/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Bratt et al., U.S. Patent No. 6,877,020 (Herein referred to as Bratt).

5. Referring to claim 1, Bratt has taught a data converter for converting a group of vectors from a time serial to a time parallel format *(i.e. matrix transposition)*, wherein in the time serial format, sets of corresponding components of the vectors each have a time slot, and in time parallel format, each vector has a time slot, the converter comprising:

an input rotator *(components that implement operation 9511 as shown in Fig. 75 and described in column 50, lines 56-62)* configured to rotate each set of corresponding

components of all vectors *(a row of elements)* by an amount that depends on the time slot *(row number)* of the set of corresponding components *[Each row of elements is rotated by an amount the depends on the row number (See Fig. 75, component 9511; column 50, lines 56-62)]*;

a bank of register files *(look up unit; See column 50, line 62 – column 51, line 4)* coupled to the input rotator to receive the rotated set of corresponding components, and having a register file *(look up table)* in the bank configured to store each rotated set of corresponding components *(column 51, lines 9-34)*;

an output rotator *(components that implement operation 9515 as shown in Fig. 75 and described in column 51, lines 5-8)* coupled to the bank of registers files *(look up unit)*, for receiving and rotating the components of a vector (*now contained in the same row)* an amount that depends on the time slot of the vector *[Each vector is rotated by an amount that depends on the row number (See Fig. 75, component 9515; column 51, lines 5-8)]*; and

a controller *(vector processor; column 52, lines 17-19)* configured to control the addressing of the bank of register files when the corresponding components of each vector are stored in a register of the bank, and to control the addressing of the bank to collect the components of each vector for subsequent output rotation *[The vector processor computes the look up table indices (i.e. controls addressing) for storing vector components into and collecting vector components from the look up unit (See Fig. 76; column 51, lines 18-34; column 52, lines 17-40)]*.

6. Referring to claim 2, Bratt has taught the data converter of claim 1, wherein

each vector *(Fig. 75, components vd0-vd7)* has n components indexed from 0 to n-1 such that there are 0 to n-1 sets of corresponding components *(Fig. 75, components va0-va7)*; and

wherein the amount of rotation by the input rotator is zero for the 0^{th} set of corresponding components *(va0)*, and n-1 steps clockwise for the $(n-1)^{th}$ set *(va7)*, any intervening sets of corresponding components being rotated by an amount equal to the ordinal number of the set *[The set of corresponding components vax is rotated right (i.e. clockwise) by x; See Fig. 75, component 9511; column 50, lines 59-62].*

7. Referring to claim 3, Bratt has taught the data converter of claim 1, wherein there are n *(8)* vectors *(Fig. 75, components vc0-vc7)* indexed from 0 to n-1; and

wherein the amount of rotation by the output rotator is zero for the 0^{th} vector and n-1 steps counter-clockwise for the (n-1)th vector, any intervening vectors being rotated by an amount equal to the ordinal number of the vector *[The vector vcx is rotated left (i.e. counter-clockwise) by x; See Fig. 75, component 9515; column 51, lines 5-8].*

8. Referring to claim 4, Bratt has taught the data converter of claim 1, wherein each register file *(look up table)* in the bank *(look up unit)* includes a register for storing the vector components *(Each look up table in the bank includes 8-bit data items (i.e. registers) that store vector components; See column 51, lines 13-18).*

9. Referring to claim 5, Bratt has taught the data converter of claim 4, wherein each vector has n components and each register file in the bank has n component registers *[Each vector has 8 components (column 51, lines 9-11) and each look up table has 256 component data items (i.e. registers) (column 51, lines 13-18)].*

10. Referring to claim 6, Bratt has taught the data converter of claim 5, wherein there are n register files in the bank *[There are 16 register files (look up tables) in the look up unit; See column 51, lines 13-15].*

11. Referring to claim 7, Bratt has taught the data converter of claim 1, wherein the bank of register files is configured to write and read the vector components at the same clock cycle *[A set of corresponding components, which is also a vector, is read from vector register va0 and written to the look up unit during cycle C1 (See cycle C1; column 53, lines 8-22, 26-28)].*

12. Referring to claim 8, Bratt has taught the data converter of claim 1, wherein the controller can alternate between horizontal writing and reading operations *(i.e. operations involving components from all different columns in the matrix)* and vertical writing and reading operations *(i.e. operations involving components from all different rows in the matrix)* on the bank of register files *[The controller alternates between horizontal and vertical read/writing to reposition elements within columns (See Fig. 75, component 9513; column 50, line 62 – column 51, line 4 & column 51, lines 19-34)].*

13. Referring to claim 9, Bratt has taught the data converter of claim 8, wherein the vector has n components and the controller horizontally writes n sets of corresponding components and horizontally reads n vectors *[8 sets of corresponding components (Fig. 75, components va0-va7), which are also vectors, are read from different columns (i.e. horizontally) in memory (Fig. 77, component 9701; column 52, lines 17-22) and written horizontally into different columns in the look up unit (Fig. 77, component 9705; column 52, lines 27-29)].*

14. Referring to claim 10, Bratt has taught the data converter of claim 9, wherein, after the controller horizontally writes n sets of corresponding components and horizontally reads n vectors, the controller vertically writes n sets of corresponding components and vertically reads n vectors *[8 vectors (Fig. 75, components vc0-vc7), which are also sets of corresponding components, are read from different rows (i.e. vertically) in the look up unit (Fig. 77, component 9707; column 52, lines 31-34) and written vertically into memory (Fig. 77, component 9711)].*

15. Referring to claim 11, Bratt has taught the data converter of claim 1, wherein the output rotator rotates the vector component a position equal and opposite to the input rotator *[The input rotator rotates vector components right (i.e. clockwise) and the output rotator rotates vector components left (i.e. counter-clockwise) by the same amount; See Fig. 75, components 9531-9534].*

16. Referring to claim 12, given the similarities between claim 1 and claim 12 the arguments as stated for the rejection of claim 1 also apply to claim 12.

17. Referring to claim 13, Bratt has taught the method of claim 12, wherein if the vector components are written horizontally to the bank of register files *(i.e. each component of the vector is written into a different column and, therefore, the vector flows horizontally)*, then the vector components are read horizontally *(i.e. from all different columns)* from the bank of register files *[When a vector is written into the look up table so that the vector flows horizontally, the vector still flows horizontally when it is read out (See Fig. 75, component 9532; column 50, line 59 – column 51, line 4)].*

18. Referring to claim 14, Bratt has taught the method of claim 12, wherein if the vector components are written vertically to the bank of register files *(i.e. each component of the vector is written into a different row and, therefore, the vector flows vertically)*, then the vector components are read vertically *(i.e. from all different rows)* from the bank of register files *[When a vector is written into the look up table so that the vector flows vertically, the vector still flows vertically when it is read out (See Fig. 75, component 9532; column 50, line 59 – column 51, line 4)]*.

19. Referring to claim 15, Bratt has taught the method of claim 12, wherein a set of corresponding components is written and the components of a vector are read in the same clock cycle *[A set of corresponding components, which is also a vector, is read from vector register va0 and written to the look up unit during cycle C1 (See cycle C1; column 53, lines 8-22, 26-28)]*.

20. Referring to claim 16, Bratt has taught the method of claim 12,

wherein the vector has n *(8)* components; and

wherein n sets of corresponding components are horizontally written over n clock cycles and vectors are horizontally read over the same n clock cycles *[8 sets of corresponding components, which are also 8 vectors, are read from vector registers va0-va7 and are written to the look up unit over the same 8 cycles. Since the vectors are written to the look up unit with each component in a different column (i.e. horizontal flow), the reads and writes are horizontal. (See cycles C1-C8; column 53, lines 8-22, 26-49)]*.

21. Referring to claim 17, Blomgren has taught the method of claim 16, wherein in another n clock cycles *(cycles C9-C16; column 53, line 50 – column 54, line 5)* subsequent to the n clock cycles *(cycles C1-C8; column 53, lines 26-49)*, n sets of corresponding components are vertically written over n clock cycles and vectors are vertically read over the same n clock cycles *[8 sets of corresponding components, which are also 8 vectors, are read from the look up unit and are written to vector registers va0-va7 over the same 8 cycles. Since the vectors are read from the look up unit with each component in a different row (i.e. vertical flow), the reads and writes are vertical. (See cycles C9-C16; column 53, lines 8-22 & column 53, line 50 – column 54, line 5)]*.

22. Referring to claim 18, given the similarities between claim 1 and claim 18 the arguments as stated for the rejection of claim 1 also apply to claim 18.

23. Referring to claim 19, given the similarities between claim 1 and claim 19 the arguments as stated for the rejection of claim 1 also apply to claim 19.

24. Referring to claim 20, given the similarities between claim 7 and claim 20 the arguments as stated for the rejection of claim 7 also apply to claim 20.

25. Referring to claim 21, given the similarities between claim 16 and claim 21 the arguments as stated for the rejection of claim 16 also apply to claim 21.

26. Referring to claim 22, given the similarities between claim 17 and claim 22 the arguments as stated for the rejection of claim 17 also apply to claim 22.

27. Referring to claim 23, given the similarities between claim 1 and claim 23 the arguments as stated for the rejection of claim 1 also apply to claim 23.

28. Referring to claim 24, Bratt has taught the data converter of claim 23, wherein the controller means is operable to control the writing and reading of the vector components to the storage means and operable to control the rotation of the vector components by the output rotation means and the input rotation means *(column 52, lines 17-40)*.

29. Referring to claim 25, given the similarities between claim 11 and claim 25 the arguments as stated for the rejection of claim 11 also apply to claim 25.

Conclusion

30. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hanounik et al. teaches a method of matrix transposing using diagonal registers.

Saulsburg et al. teaches an apparatus for performing a matrix transpose on vector registers.

Jung et al. teaches an apparatus for performing a matrix transpose using register file that is accessed both row-wise and column-wise.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

3/1/06

HENRY W. H. TSAI
PRIMARY EXAMINER